CLAIMS:

What is claimed is:

1. A semiconductor package comprising:

a substrate;

a first die on and electrically coupled to the substrate;

a support structure on the substrate over the first die;

a second die on the support structure over the first die and electrically coupled to the substrate; and

a hardened unitary body of an encapsulant material covering the first die, the support structure, and the second die, wherein the encapsulant material is vertically between the first die and the second die.

2. The semiconductor package of claim 1, wherein the support structure is thermally coupled to a heat sink of the substrate.

3. The semiconductor package of claim 1, wherein a portion of the support structure is electrically conductive and said portion is electrically coupled between the substrate and the second die.

4. The semiconductor package of claim 1, wherein the support structure includes a first surface and an opposite second surface that faces the first die, the first surface of the support structure includes a central recess, and the second die is in the recess.

5. The semiconductor package of claim 1, wherein the support structure includes horizontally extending feet, said feet being mounted on a conductive region of the substrate.

6. The semiconductor package of claim 1, wherein the support structure is electrically coupled to an internal electrically conductive layer of the substrate located between a first surface of the substrate on which the first die is mounted and an opposite second surface.

7. The semiconductor package of claim 1, wherein the support structure comprises a circuit film having conductive traces thereon, and the second die is electrically coupled to the substrate through the conductive traces.

8. The semiconductor package of claim 7, wherein the support structure includes a first surface and an opposite second surface that faces the first die, the first surface of the support structure includes a central recess, and the second die is in the recess.

9. The semiconductor package of claim 8, wherein the second semiconductor die is in a flip chip connection with the circuit film.

10. The semiconductor package of claim 9, wherein the support structure includes a first surface and an opposite second surface that faces the first die, the circuit film is on the first surface of the support structure, and the second die is electrically coupled to the circuit film.

11. The semiconductor package of claim 10, wherein the second semiconductor die is in a flip chip connection with the circuit film.

12. The semiconductor package of claim 1, wherein the support structure comprises a rigid metal leadframe including leads, and the second die is electrically connected to respective ones of the leads.

13. The semiconductor package of claim 12, wherein the metal leadframe includes a central die pad on which the second die is mounted.

14. The semiconductor package of claim 12, wherein the metal leadframe comprises at least one layer of a nonconductive tape interconnecting a plurality of the leads.

15. The semiconductor package of claim 1, wherein the first die is electrically coupled to the substrate by bond wires, and said wires extend through one or more apertures in the support structure.

16. The semiconductor package of claim 1, wherein the first die is electrically connected to the substrate by bond wires, and a point of connection between the bond wires and the substrate is outside a perimeter of the support structure.

17. The semiconductor package of claim 16, wherein the support structure includes a first surface and an opposite second surface that faces the first die, the first surface of the support structure includes a central recess, and the second die is in the recess.

18. A semiconductor package comprising:

a substrate having a first surface;

a first die on and electrically connected to the first surface of the substrate;

a second die in a flip chip connection with the first die;

a thermally conductive first structure having an internal cavity and superimposing the first and second dies, said first structure being thermally coupled to the substrate, and thermally coupled by a thermally conductive layer to the second die;

a unitary body of a hardened encapsulant covering the first and second dies and filling the internal cavity of the first structure.

19. The semiconductor package of claim 18, wherein the first die is electrically coupled to the substrate by bond wires, and a point of connection of the bond wires to the substrate is outside of a perimeter of the first structure.

20. The semiconductor package of claim 18, wherein the support structure is electrically coupled to an internal electrically conductive layer of the substrate located between a first surface of the substrate on which the first die is mounted and an opposite second surface.

21. A semiconductor package comprising:

a substrate;

a first die electrically coupled to the substrate;

a second die electrically coupled to the substrate and superimposed over the first die; and

a heat spreader disposed between the first and second dies, thermally coupled to the first and second dies by respective thermally conductive layers, and thermally coupled to the substrate; and

a unitary body of a hardened encapsulant covering the first and second dies and filling an internal cavity of the heat spreader.

22. The semiconductor package of claim 21, wherein the first die is electrically coupled to the substrate in a flip chip connection.

23. The semiconductor package of claim 23, wherein the second die is electrically coupled to the substrate through apertures in the heat spreader.

24. The semiconductor package of claim 21, wherein the second die is electrically coupled to the substrate by bond wires that extend through apertures in the heat spreader.

25. The semiconductor package of claim 21, wherein the first and second dies are electrically coupled to the substrate by conductive wires.

26. The semiconductor package of claim 21, further comprising a second heat spreader superimposed over the first and second dies, and thermally coupled between the second die and the substrate.

27. The semiconductor package of claim 26, wherein the second heat spreader is thermally coupled to an active surface of the second die.

28. The semiconductor package of claim 27, wherein the first die is electrically coupled to the substrate in a flip chip connection.